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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,297	09/08/2003	Hiroyuki Sekine	Q75815	8677

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EXAMINER	
EISEN, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,297	SEKINE, HIROYUKI	
	Examiner	Art Unit	
	Alexander Eisen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-51* is/are allowed.

6)☒ Claim(s) *1-3,5-7,15-18 and 20-22* is/are rejected.

7)☒ Claim(s) *4,8-14,19 and 23-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 1 is objected to because of the following informalities: claim recites: "wherein said data driver circuit ***comprises*** by N switching blocks", which probably should read "wherein said data driver circuit ***is comprised*** by N switching blocks", or "wherein said data driver circuit ***comprises*** ~~by~~ N switching blocks".

Claim 1 also recites in the last line on page 64 "said M video signal wirings", which apparently should read simply "M video signal wirings" since there is no antecedent basis for "said M video signal wirings".

Claim 1 also recites in the first line on page 65 "the M switching elements", and "the M video signals" in the 9th line on page 65, which apparently should read "M switching elements" and "M video signals".

3. Claim 5 is objected to because of the following informalities: claim 5 recites "□said M video signal wirings" on line 15, page 67, which apparently should read "M video signal wirings" since no particular M signal wirings was mentioned before, namely there is no antecedent basis for such limitation.

Claim 5 further recites "□said M video signal wirings of an i-th set (one of i = 1, 2, …, P) of 2M video signal wirings". It is noted that it is only two sets of M wirings, since the total

number is 2M, and therefore there is no point to claim i = 1, 2, ..., P. There are no sets beyond i = 2.

4. Claim 38 is objected to because of the following informalities: claim 38 recites: "the switch block " in the fourth line. There is no antecedent basis for such limitation.

Appropriate corrections is are required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-7, 15-18 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Kanno et al., US 4,779,086, hereinafter Kanno.

With respect to claim 1 Kanno discloses a liquid crystal display device driving method wherein said liquid crystal display device comprises a pixel matrix (FIGS. 3-4) having pixels including gate lines Gn, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines; a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period; a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period; a matrix substrate on which said data driver circuit and said gate driver circuit are formed; a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode 12 common to all said pixels on said matrix substrate is

arranged; wherein said data driver circuit comprises by N switching blocks (16 switching block are shown in FIG. 1; B1-FIRST, B1-LATTER ...B8-LATTER, i.e. N=16) each having M (each B-block has 120; S1 – S120 and S121-S240; i.e. M=120) switching elements (TFT transistors S), a scanning circuit for outputting an open/close control signal for each switching block (B-TFT GATE DRIVER in FIG. 3), and MxP (D1-D240; total MxP = 120X2; i.e. P=2, natural number) video signal wirings forming one set of said MxN video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set; M video signal wirings of an i-th set (one of i=1, 2, . . . , P) of the MxP video signal pairings are respectively connected to input terminals of the M switching elements of the i-th switching block, when viewed from the first switching block; and wherein said data lines are divided into blocks each having M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M switching elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block, said driving method comprising: an outputting step wherein said scanning circuit outputs the open/close control signal synchronously with the M video signals supplied successively every P sets, and successively outputs every set of the P sets simultaneously within the set through the MxP video signal wirings in an arbitrary horizontal time period, a sampling step wherein the M video signals, which are supplied successively every P sets, successively every set of the P sets and simultaneously within the set, are sampled to the M data lines connected to the M switching elements so as to simultaneously conduct in the M switching elements of the

switching block (see timing diagram in FIG. 2; col. 2, lines 30-51; col. 3, line 42 – col. 4, line 47).

As pertaining to claim 2, the driving method further comprises a writing step wherein the M (120) video signals (D1-D120) that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors (as in FIG. 4), and are caused to simultaneously conduct through the M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines (G_{n-2}, G_{n-1} and G_n, as in FIG. 4) through which the gate driver circuit (as in FIG. 3) supplies the gate signal during the arbitrary horizontal time period and which simultaneously conduct.

As pertaining to claim 3, Kanno further discloses that at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the scanning circuit to the switching block in which the M switching elements simultaneously conduct subsequent to M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit (as can be seen from the timing diagram in FIG. 2 the open/close control signals B are supplied sequentially to subsequent blocks of switching elements causing the latter to conduct after the previously conducting group conducting state elapses).

Claims 5-7 are directed to a similar invention as in claims 1-3 with the only exception that the number of signal wirings is limited to two. Kanno discloses such arrangements and therefore claims 5 through 7 are rejected on the same grounds as claims 1-3.

As pertaining to claim 15, Kanno discloses a liquid crystal display device (FIGS. 3-4; see also relevant discussion of claim 1) comprising a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines; a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period; a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period; a matrix substrate on which said data driver circuit and said gate driver circuit are formed; a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged; wherein said data driver circuit comprises by N (N=16) switching blocks each having M (M=120) switching elements, a scanning circuit for outputting an open/close control signal B1-B8 for each switching block, and MxP (P is a natural number) video signal wirings forming one set of said MxN (1920) video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set; said M video signal wirings of an i-th set (one of i=1, 2, . . . , P) of the MxP video signal wirings are respectively connected to input terminals of the M switching elements of the i-th switching block; wherein said data lines are divided into blocks each having M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M switching

elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block, wherein the scanning circuit outputs the open/close control signal B synchronously with the M video signals supplied successively every P sets (see FIG. 2), and successively outputs every set of the P sets simultaneously within the set through the MxP video signal wirings in an arbitrary horizontal time period.

As pertaining to claim 16, Kanno further discloses the liquid crystal display device, wherein M video signals (M=120), which are supplied successively every P sets (P=2), successively every set of the P sets and simultaneously within the set, are sampled to the M data lines connected to the M switching elements which simultaneously conduct in the M switching elements of the switching block (see FIG. 2 and relevant description).

As pertaining to claim 17, Kanno further teaches the liquid crystal display device, wherein the M (M=120) video signals that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors which simultaneously conduct through the M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines through which the gate driver circuit supplies the gate signal during the arbitrary horizontal time period and which simultaneously conduct.

As pertaining to claim 18, Kanno further teaches that at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from

the scanning circuit to the switching block in which the M switching elements simultaneously conduct on the heels of M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit (see discussion of relevant method claims 3 and 7 containing similar subject matter).

As pertaining to claim 20, Kanno discloses a liquid crystal display device (FIGS. 3-4) comprising a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between said gate lines and said data lines; a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period; a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period; a matrix substrate on which said data driver circuit and said gate driver circuit are formed; a liquid crystal sandwiched between said matrix substrate and a counter substrate on which a counter electrode common to all said pixels on said matrix substrate is arranged; wherein said data driver circuit comprises by N (N=16) switching block each having M switching elements, a scanning circuit for outputting an open/close control signal for each switching block, and 2M (2x120=240) video signal wirings forming one set of said MxN video signals from said video signal corresponding to a first pixel time period up to said video signal corresponding to a final pixel time period within the horizontal time period as one set; said M video signal wirings of an i-th set (one of i=1, 2, . . . , P) of the 2M video signal wirings are respectively connected to input terminals of the M switching elements of the i-th switching block; wherein said data lines are divided into blocks each having said M data lines, wherein said M data lines of each block are respectively connected to output terminals of said M

switching elements within each of the switching blocks from a first switching block up to a final switching block of the N switching blocks defined in blocks from a first block up to a final block, wherein the scanning circuit outputs the open/close control signal synchronously with the M video signals supplied successively every two sets, and successively outputs every set of the two sets simultaneously within the set through the 2M video signal wirings in an arbitrary horizontal time period.

As pertaining to claim 21, Kanno further discloses the liquid crystal display device, wherein the M video signals, which are supplied successively every two sets, successively every set of the two sets and simultaneously within the set, are sampled to the M data lines (by signals b), connected to the M switching elements which are caused to simultaneously conduct in the M switching elements of the switching block.

As pertaining to claim 22, Kanno further discloses the liquid crystal display device, wherein the M video signals that are sampled individually are respectively written to the M pixels of the set including the M pixel transistors which simultaneously conduct through the M pixel transistors of the set every set of M pixel transistors which are connected to the gate lines G_n through which the gate driver circuit supplies the gate signal during the arbitrary horizontal time period and which simultaneously conduct.

Allowable Subject Matter

7. Claims 4, 8-14, 19 and 23-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: none of the prior art, either singularly or in combination, teach or fairly suggest a liquid crystal display device or a method of driving the same, wherein the M video signals supplied through the M video signal wirings for each set of the P sets are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period, or, wherein at a time instant when a first time period of a conduction time period when each of the M switching elements is in the conducting state elapses from a time instant of start of the conduction of the M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit, the open/close control signal is supplied from the scanning circuit to the switching block in which the M switching elements simultaneously conduct subsequent to M switching elements of the switching block which are formerly caused to simultaneously conduct with the open/close control signal supplied from the scanning circuit; and wherein the M video signals supplied through the M video signal wirings for each set of the P sets are the video signals the polarity of which is changed with respect to the counter electrode between the first time period and a second time period as the remaining time period of the conduction time period following the first time period.

9. Claims 36-51 are allowed.

10. The following is an examiner's statement of reasons for allowance: none of the prior art have been found that suggested a modification of or a combination with the cited prior art so as to arrive to the combination of the limitations of independent claims 36, 37, 44 and 45; namely, a

a liquid crystal display device and driving method thereof, wherein the liquid crystal display device comprises a pixel matrix having pixels including gate lines, data lines disposed orthogonally to said gate lines, and pixel transistors arranged at intersections between the gate lines and said data lines; a data driver circuit for supplying video signals from a video signal corresponding to a first pixel time period up to a video signal corresponding to a final pixel time period to different data lines every horizontal time period; a gate driver circuit for supplying a gate signal to a corresponding gate line every horizontal time period; a matrix substrate on which the data driver circuit and said gate driver circuit are formed; a liquid crystal sandwiched between the matrix substrate and a counter substrate on which a counter electrode common to all the pixels on the matrix substrate is arranged; wherein the data driver circuit is comprised by video signal wirings through which the video signals from the video signal corresponding to the first time period up to the video signal corresponding to the final time period are adapted to be supplied every horizontal time period; switching elements for connecting the video signal wirings to the data lines to which the video signals are to be respectively supplied; and a scanning circuit for outputting an open/close control signal in accordance with which the switching elements are caused to conduct, the open/close control signal being supplied from the scanning circuit to the switching elements to which the video signals are supplied synchronously with the video signals supplied through the video signal wirings, respectively, said driving method comprising: a step of supplying wherein the video signals supplied through the video signal wirings being sampled to the data lines to which the video signals are to be supplied in the switching elements which are caused to conduct with the open/close control signal, and a step of sampling wherein the sampled video signals being passed through the pixel transistors which are

connected to the gate line through which the gate signal is adapted to be supplied by the gate driver circuit and which are caused to conduct to be written to the pixels including the pixel transistors, respectively, for a supply horizontal period when the video signals are supplied to the video signal wirings, respectively, wherein the video signals which are to be supplied to the video signal wirings to which the switching elements caused to conduct in accordance with the open/close control signal are connected are the video signals the polarity of which is changed with respect to the counter electrode between the first time period, which is in a conduction time period when the switching elements are caused to conduct with the open/close control signal, and a second time period as the remaining time period of the conduction time period following the first time period.

Karube et al., UD 6,414,668 B1, discloses block based driving circuit with opposite polarity driving signals.

Jeong, US 6,008,801, discloses reversal polarity driving circuit for a display device having 6x3 video signal wiring and inverting polarity for Examiner respectfully disagrees.=ach sequential 6 wirings.

None of the above discloses the feature, wherein the video signals which are to be supplied to the video signal wirings to which the switching elements caused to conduct in accordance with the open/close control signal are connected are the video signals the polarity of which is changed with respect to the counter electrode between the first time period, which is in a conduction time period when the switching elements are caused to conduct with the open/close control signal, and a second time period as the remaining time period of the conduction time period following the first time period.

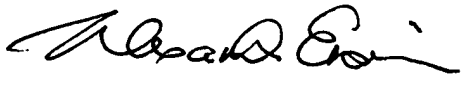
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander Eisen
Primary Examiner
Art Unit 2674

16 March 2006